REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on September 4, 2003, and the references cited therewith.

Claim1 is amended, no claims are canceled, and claims 64-73 are added; as a result, claims 1-3 and 64-73 are now pending in this application.

Information Disclosure Statement

Applicant submitted an Information Disclosure Statement and a 1449 Form on December 14, 2003. Applicant respectfully requests that initialed copies of the 1449 Form be returned to Applicants' Representatives to indicate that the cited references have been considered by the Examiner.

Affirmation of Election

As provisionally elected by Applicants representative, Daniel J. Kluth, on September 23, 2003, Applicant elects to prosecute the invention of Group I, claims 1-3.

The claims of the non-elected invention, claims 25, 47, 55-59, and 61 (Groups II-IV), are hereby canceled. However, Applicant reserves the right to later file continuations or divisions having claims directed to the non-elected inventions.

§103 Rejection of the Claims

Claims 1-3 were rejected under 35 USC § 103(a) as being unpatentable over Yamada et al. (U.S. 5,617,537).

The rejection stated that Yamada shows, "a local address storage circuitry which stores a local address for identifying the storage circuitry's single associated memory device once the address assign command is decoded by the command decoder (the local address, as well as the addresses of other devices, is stored in each PM in map area 21M)."

Yamada appear to show a number of processor modules 18-1, 18-2, 18-3, each including processors 19-1, 19-2, 19-3. Yamada also appears to show a map area 21M on each of the processor modules. However, Applicant is unable to find in Yamada, a plurality of memory devices associated with one processor, wherein each memory device includes a local address

storage circuitry which stores a local address for identifying the storage circuitry's single associated memory device once an address assign command is decoded by a command decoder.

In contrast, claim 1 as amended includes a plurality of memory devices associated with one processor, wherein each memory device includes a local address storage circuitry which stores a local address for identifying the storage circuitry's single associated memory device once an address assign command is decoded by a command decoder. Because Yamada does not show or make obvious every element of Applicant's independent claims, a 35 USC § 103(a) rejection is not supported by the references. Reconsideration and withdrawal of the rejection is respectfully requested with respect to amended claim 1. Additionally, reconsideration and withdrawal of the rejection is respectfully requested with respect to claims 2 and 3 that depend therefrom as depending on allowable base claims.

Applicant has added claims 64-73 to further define the scope of Applicant's invention. Applicant respectfully submits that claims 64-73 are in condition for allowance.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 373-6944) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743

Respectfully submitted,

ROBERT D. NORMAN

By his Representatives,

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Date 12-4-2003

By _____
David C. Peterson
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 4th day of December, 2003.

Amy Moriarty
Name

_____
Signature